

Fig. 1

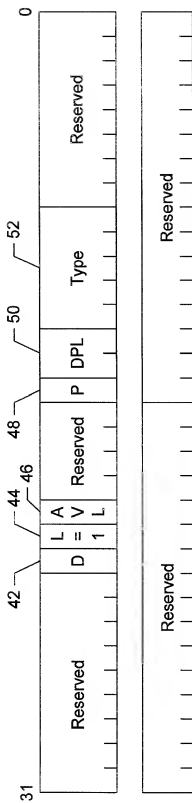


Fig. 2

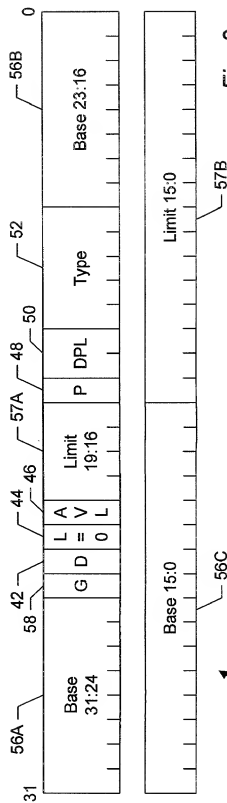


Fig. 3

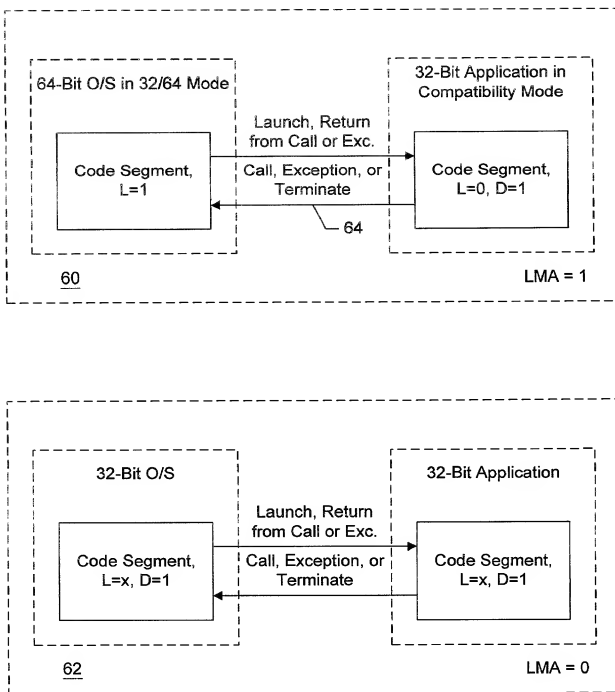


Fig. 4

<u>LMA</u>	<u>CS L Bit</u>	<u>CS D Bit</u>	<u>Operating Mode</u>
0	x	0	16 Bit Mode
0	x	1	32 Bit Mode
1	0	0	16 Bit Compatibility Mode
1	0	1	32 Bit Compatibility Mode
1	1	0	32/64 Mode
1	1	1	Reserved

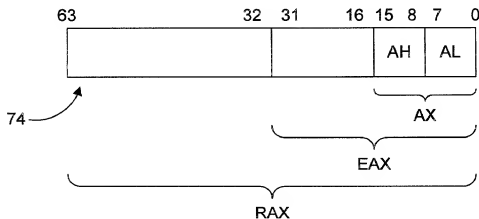
70

Fig. 5

<u>Override Prefix</u>		<u>None</u>	<u>REX</u>	<u>(66H , 67H)</u>
32/64 Mode	Operand Size	32 bits	64 bits	16 bits
	Address Size	64 bits	DNA	32 bits
32 Bit Mode Incl. Compatibility Mode	Operand Size	32 bits	DNA	16 bits
	Address Size	32 bits	DNA	16 bits
16 Bit Mode Incl. Compatibility Mode	Operand Size	16 bits	DNA	32 bits
	Address Size	16 bits	DNA	32 bits

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Fig. 6



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Fig. 7

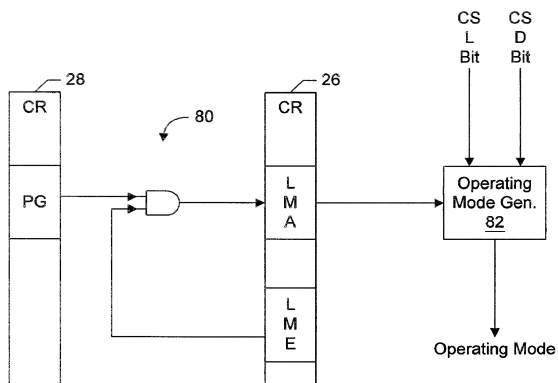


Fig. 8

<u>Change</u>	<u>Check</u>
LME 0 \rightarrow 1	If PG=1 then exception
LME 1 \rightarrow 0	If PG=1 then exception
PG 0 \rightarrow 1	If LME=1 and PAE=0 then exception
PAE 1 \rightarrow 0	If LMA=1 then exception

90 *Fig. 9*

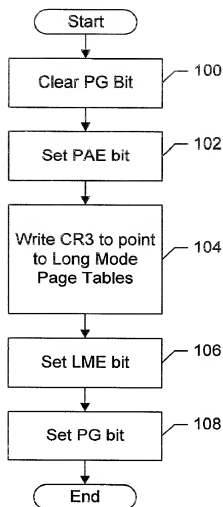


Fig. 10

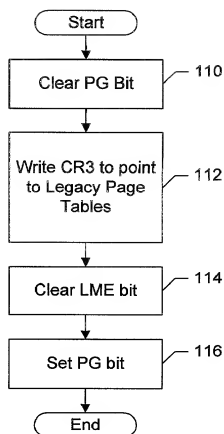


Fig. 11

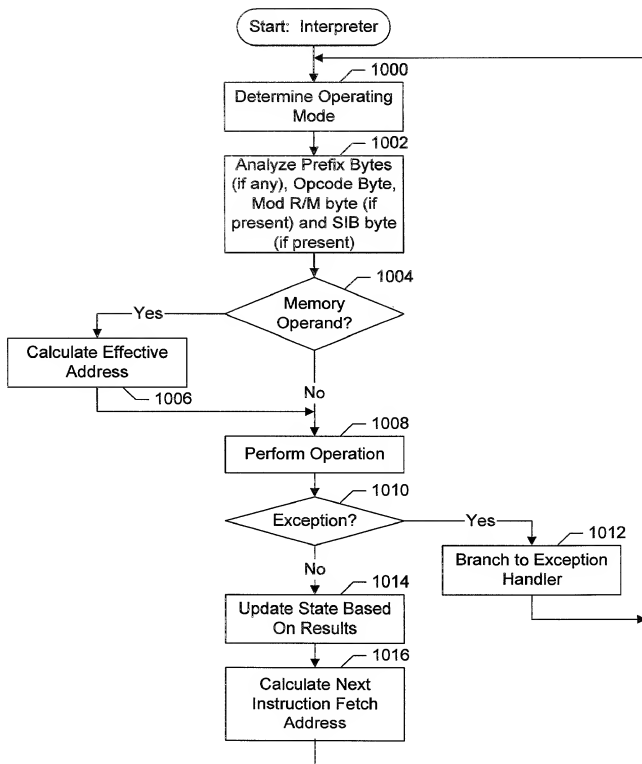


Fig. 12

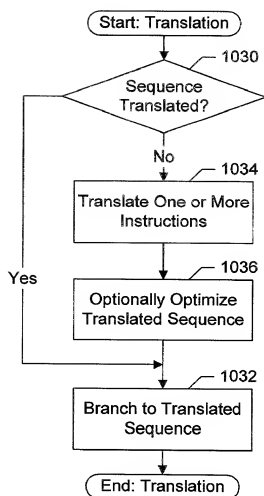


Fig. 13

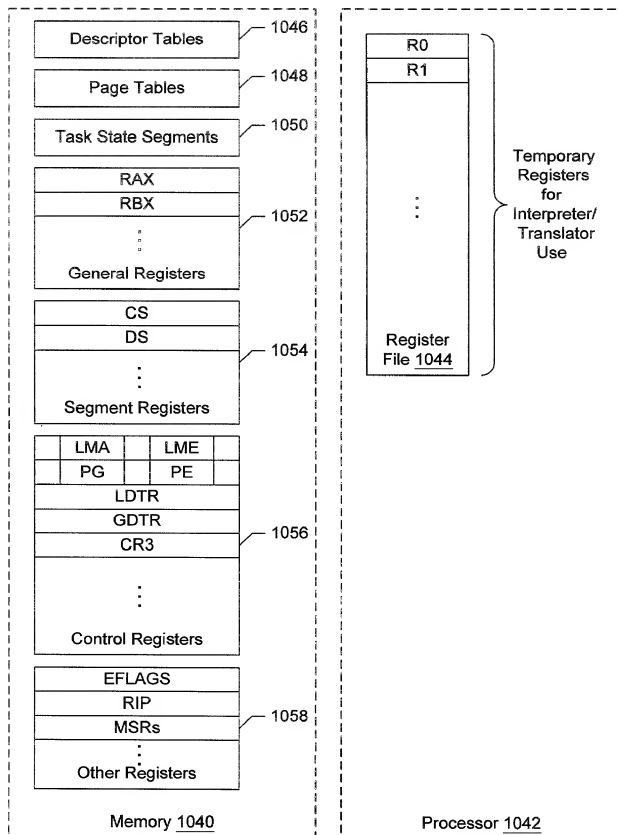


Fig. 14

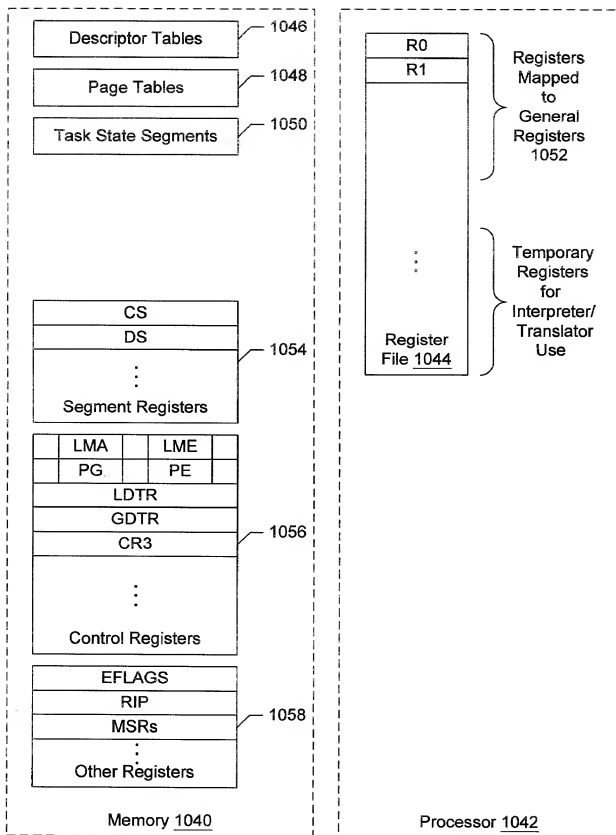


Fig. 15

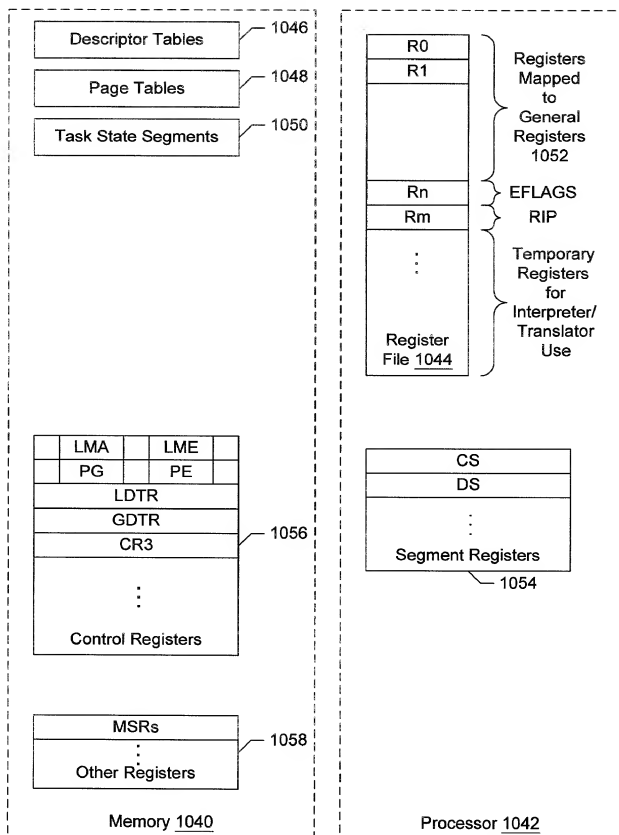


Fig. 16

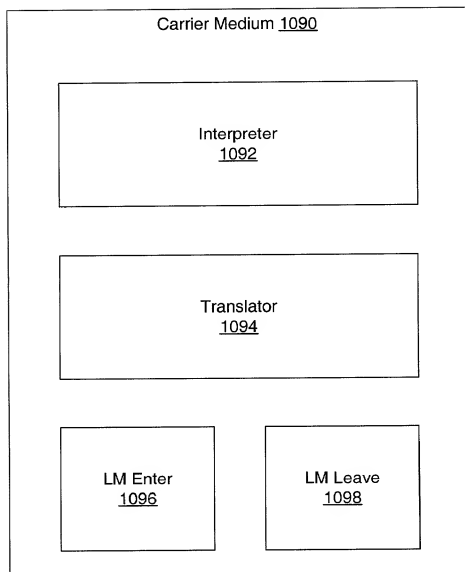


Fig. 17

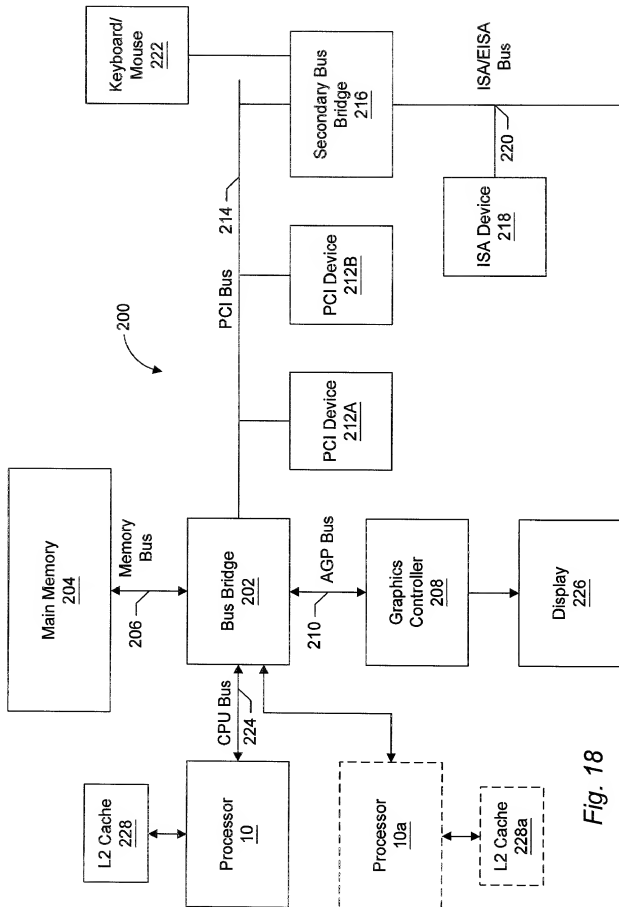


Fig. 18

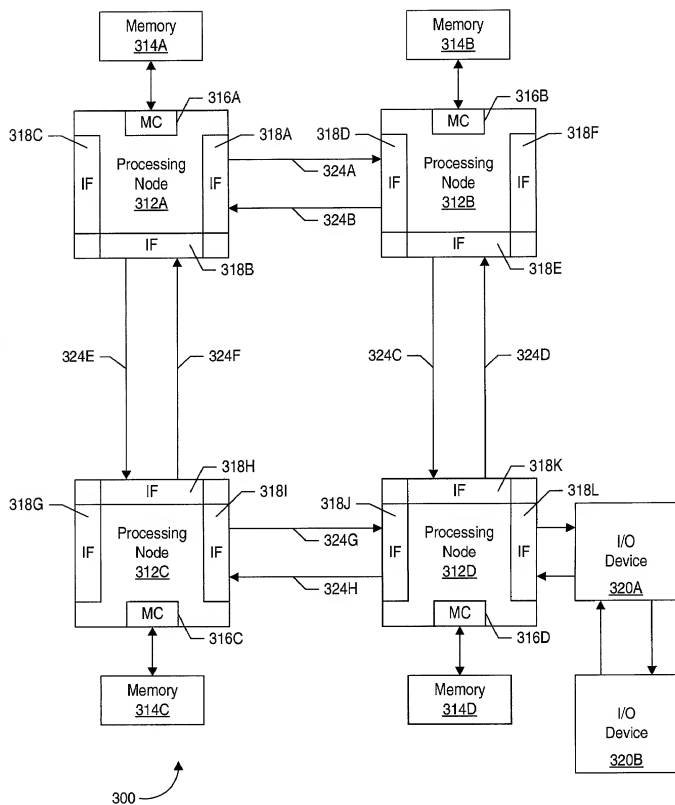


Fig. 19